Electronic Version
Stylesheet Version v1.1.1

EEPROM WITH SOURCE LINE VOLTAGE STABILIZATION MECHANISM

Abstract

A low-voltage nonvolatile memory array includes an N type semiconductor substrate having a memory region. A deep P well is formed in the semiconductor substrate. A cell N well is located within the memory region in the semiconductor substrate. The cell N well is situated above the deep ion well. A shallow P well serving as a buried bit line is doped within the cell ion well. The shallow P well is isolated by an STI layer, wherein the STI layer has a thickness greater than a well depth of the shallow ion well. At least one memory transistor with a stacked gate, a source, and a drain is formed on the shallow ion well. The source of the memory transistor is electrically coupled to the cell N well to induce a capacitor between the cell N well and the deep P well during a read operation, thereby avoiding read current bounce or potential power crash. A bit line overlies the memory transistor and is electrically connected to the drain of the memory transistor via a bit line contact plug short-circuiting the drain of the memory transistor and the shallow P well.